PATENT ABSTRACTS OF JAPAN

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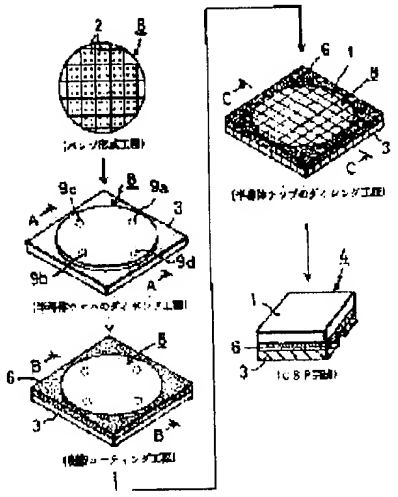
(54) MANUFACTURE OF CHIP-SIZED PACKAGE

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain a chip-sized package in which a process up to a semiconductor package from the formation of a bump is reduced and whose alignment in a die bonding operation is made easy by a method wherein the gap between a semiconductor wafer which is die-bonded by the bump and a circuit board is sealed with a resin and the circuit board and the semiconductor wafer are diced into individual semiconductor chips.
SOLUTION: Many bumps 2 which are lined up on a semiconductor wafer 8 are formed, the semiconductor wafer 8 is turned over, the bumps 2 are directed downward, the semiconductor wafer is placed on a circuit board 4, and it is positioned in four upper and lower as well as right and left points 9a, 9b, 9c, 9d so as to be die-bonded. Then, this assembly is passed through a reflow furnace, and the bumps 2 are melted so as to be bonded onto the circuit board 3. Then, a resin 6 is filled into the gap between the semiconductor wafer 8 and the circuit board 3, the bumps 2 are sealed, and this assembly is passed through a curing furnace so as to be hardened. Then, the semiconductor wafer 8 is cut in square shapes so as to be divided into individual semiconductor chips 1 by a dicing machine. At this time, also the circuit board 3 is diced together with the semiconductor chips 1.



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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the manufacture technique of a semiconductor package, especially relates to the manufacture technique of a micro chip size package.
[0002]
[Description of the Prior Art] In recent years, in connection with a miniaturization of a set device, the microminiaturization of a semiconductor package progresses increasingly, and, recently, the so-called chip size package (CSP) which used bump connection technique is developed (refer to electronics package technical 1995 (Vol.11 No.3) and JP,6-349893,A). As shown in drawing 10 , as many bumps 2 are formed in the inferior surface of tongue of a semiconductor chip 1, a semiconductor chip 1 is directly mounted on a mother board, and circuit connection of the bump 2 is made or it was shown in drawing, a bump 2 is connected to the circuit board 3 of the same configuration as a semiconductor chip 1, it considers as the stratified semiconductor package 4, and this connects to a mother board the electrode 5 prepared in the inferior surface of tongue of the circuit board 3. In addition, the opening between the semiconductor chips 1 and the circuit boards 3 which are formed of a bump 2 is closed with the resin 6.
[0003] Drawing 11 shows the 1 manufacturing-process view of the semiconductor package 4 (CSP) which consists of above-mentioned structure. In this manufacturing process, after having formed the integrated circuit on wafers, such as silicon, first, considering as the semiconductor wafer 8, giving the passivation layer to the front face and protecting an integrated circuit, the bump 2 of the masses which aligned on the semiconductor wafer 8 is formed. At the following process, the dicing of the semiconductor wafer 8 is carried out for every semiconductor chip, and the spacing of semiconductor chip 1 comrades which adjoin according to an expanded process is vacated so that it may further be easy to adsorb a semiconductor chip 1 a piece every. At the following process, the semiconductor chip 1 which carried out [above-mentioned] expanded is arranged a piece every using an adsorption nozzle in the predetermined position of the circuit board 3 formed with glass epoxy or the film. As shown in drawing 12 , a semiconductor chip 1 turns a bump 2 to the bottom, is arranged by the circuit board 3, and carries out die bonding of the bump 2 on a predetermined electronic circuitry. Melting of the bump 2 is carried out at a reflow process, and it joins on the circuit board 3. The following resin coating process is for closing the opening between a semiconductor chip 1 and the circuit board 3, and it fills up with a resin 6 among both. A resin 6 is hardened by letting cure kiln pass. At the last dicing process, with a dicing machine, it cuts a measure ** and considers as the semiconductor chip 1 of every a piece. At this time, the dicing also of the circuit board 3 is carried out together with a semiconductor chip 1, and the semiconductor package 4 (CSP) of a rectangular parallelepiped configuration completes it.
[0004]
[Problem(s) to be Solved by the Invention] However, if it is in the above-mentioned conventional manufacture technique, when six processes were needed by completion of the semiconductor package 4 from a bump's 2 formation, the semiconductor chip 1 was transported on the piece [every] circuit board 3, and after carrying out position doubling about each, there was a problem that the routing is troublesome, and also that die bond must be carried out etc. will require working hours.
[0005] Then, this invention offers the manufacture technique of the chip size package which enabled it to perform position doubling in a die bond process etc. easily at the same time it reduces the manufacturing process from a bump's formation to completion of a semiconductor package.
[0006]
[Means for Solving the Problem] In order to solve the above-mentioned technical probrem, namely, the manufacture technique of the chip size package concerning this invention The process which forms a bump on a semiconductor wafer the 1st, and the process which carries out die bond of the semiconductor wafer on the circuit board by this bump, The process which carries out the resin seal of between the semiconductor wafers and the circuit boards which carried out die bond, The process which is characterized by having the process which carries out the dicing of the circuit board which carried out the resin seal, and the semiconductor wafer for every semiconductor chip, and forms a bump on a semiconductor wafer the 2nd, The process which carries out die bond of the semiconductor wafer on the circuit board by this bump, The process which carries out the dicing only of the semiconductor wafer which the circuit board left and carried out die bond for every semiconductor chip, It is characterized by having the process which carries out the dicing of the process which carries out the resin seal of between the semiconductor wafers and the circuit boards which carried out dicing on the circuit board, and the circuit board which carried out the resin seal

and a semiconductor wafer for every semiconductor chip.
[0007]
[Embodiments of the Invention] Hereafter, the manufacture technique of the chip size package which relates to this invention based on an accompanying drawying is explained in detail. Drawing 1 shows the manufacturing process of the first example of this invention. After having formed the integrated circuit on wafers, such as silicon, first, considering as the semiconductor wafer 8 like a previous example, giving the passivation layer to the front face and protecting an integrated circuit, the bump 2 of the masses which aligned on the semiconductor wafer 8 is formed. Next, the above-mentioned semiconductor wafer 8 is turned over, a bump 2 is turned to the bottom, it lays on the circuit board 3 as it is, and after die bond is positioned and carried out on the four vertical and horizontal points 9a, 9b, 9c, and 9d (refer to the drawing 2). Next, melting of the bump 2 is carried out to a reflow through this, and it joins on the circuit board 3. The following resin coating process is for closing the opening between the semiconductor wafer 8 and the circuit board 3. As shown in drawing 3 , the opening between both is filled up with a resin 6, and a bump 2 is closed. A resin 6 is hardened by letting it pass at cure kiln. At the following dicing process, with a dicing machine, the semiconductor wafer 8 is cut a measure ** and divided for every semiconductor chip. At this time, as shown in drawing 4 , the dicing also of the circuit board 3 is carried out together with a semiconductor chip 1, and it is completed as a semiconductor package 4 (CSP) of a rectangular parallelepiped configuration.
[0008] Thus, in the above-mentioned example, since die bond is carried out on the circuit board 3 in the state of the semiconductor wafer 8 unlike the conventional example, the process which carries out expanded [of the process which carries out the dicing of the semiconductor wafer 8 before carrying out die bond to the circuit board 3 like before, and the semiconductor chip 1 which carried out dicing] is omissible. Moreover, compared with performing a die bond process at a time one piece of the semiconductor chips like before repeatedly, since only 1 time is required, it can manufacture at four few processes two processes conventionally, and also position doubling work of the semiconductor wafer 8 in a die bond process becomes very easy.
[0009] Drawing 5 shows the manufacturing process in the second example of this invention. In this example, since the process which forms a bump 2 on the semiconductor wafer 8, and the process which carries out die bond of the semiconductor wafer 8 on the circuit board 3 are the same as the first aforementioned example, a detailed explanation of each process is omitted. In this example, to the semiconductor wafer 8 by which die bond was carried out on the circuit board 3, as shown in drawing 6 , the process which leaves the circuit board 3 as it is, carries out the dicing only of the semiconductor wafer 8 for every chip, and is made into the semiconductor chip 1 of a measure ** differs from a previous example. Although the following resin coating process is like the above-mentioned for carrying out the resin seal of the opening between the semiconductor wafer 8 and the circuit board 3, a resin 6 is filled up with this example also not only into the opening between the semiconductor wafer 8 and the circuit board 3 but into the opening between semiconductor chip 1 comrades which carried out dicing as shown in drawing 7 . After stiffening a resin 6 at cure kiln, again, along with the dicing line of a semiconductor chip 1, the dicing also of the circuit board 3 is carried out together (refer to the drawing 8), and it completes the semiconductor package 4 (CSP) of a rectangular parallelepiped configuration shortly.
[0010] Thus, since die bond is carried out on the circuit board 3 in the state of the semiconductor wafer 8 unlike the conventional example even if it is in the second example The dicing process and expanded process of a semiconductor wafer 8 like before are omissible. It can manufacture at five few processes one process conventionally, and also since the resin is filled up with this example after carrying out the dicing of the semiconductor wafer 8 on the circuit board 3 and making it a semiconductor chip 1, in it, it is effective in a resin seal becoming an authenticity much more. Moreover, when dicing width of face of the two-times scale division cut together with the circuit board 3 was made narrower than the first dicing width of face which cuts only the semiconductor wafer 8, as it was shown in drawing 9 , it can leave a resin 6 to the periphery of the side face of a semiconductor chip 1, and is effective in the ability to protect a semiconductor chip 1 to an authenticity more by this.
[0011]
[Effect of the Invention] As explained above, since die bond is carried out on the circuit board in the state of a semiconductor wafer, according to the manufacture technique of the chip size package concerning this invention, position doubling work of a up to [the circuit board at the time of carrying out die bond] becomes very easy compared with carrying out for every semiconductor chip like before, and also the effect that it can manufacture with the number fewer than the conventional manufacturing process of processes is done so.
[0012] Moreover, after carrying out die bond of the semiconductor wafer on the circuit board, when the dicing only of the semiconductor wafer is carried out to a measure ** and it considers as a semiconductor chip, the effect that a resin seal becomes a much more positive thing is acquired.

[Translation done.]